

WHAT IS CLAIMED, IS:

1. Method for pre-processing input signals of interfaces of different type for common-format central processing, using a common system clock, said different interface types being associated with differing sample clock frequencies and/or differing data frame or data word formats, said method including the steps:
 - generating from the different-type interface input signals system clock synchronised input signals;
 - channel decoding said system clock synchronised input signals according to the differing channel protocols related to said different-type interfaces, thereby providing corresponding PCM bitstream format signals having a uniform word format;
 - further processing said PCM bitstream format signals so as to form therefrom sample words that are stored in an intermediate store, e.g. a FIFO, from which the sample words are fed to said central processing.
2. Method for pre-processing output signals for interfaces of different type in a common-format central processing using a common system clock, said different interface types being associated with differing sample clock frequencies and/or differing data frame or data word formats, said method including the steps:
 - further processing sample words that were output from said central processing and stored in an intermediate store, e.g. a FIFO, by forming system clock synchronised PCM bitstream format signals therefrom, which PCM bitstream format signals have a uniform word format and are related to said interfaces of different type;
 - channel encoding said system clock synchronised PCM bitstream format signals having a uniform word format according to the differing channel protocols related to said different-type interfaces, thereby providing corre-

- sponding system clock synchronised output signals;
- generating from said system clock synchronised output signals interface-type related output signals (SADO) that are no more system clock synchronised but conform to said type of interface.
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3. Apparatus for pre-processing input signals of interfaces of different type for common-format central processing, using a common system clock, said different interface types being associated with differing sample clock frequencies and/or differing data frame or data word formats, said apparatus including:
- means for generating from the different-type interface input signals system clock synchronised input signals;
 - 10 - means for channel decoding said system clock synchronised input signals according to the differing channel protocols related to said different-type interfaces, thereby providing corresponding PCM bitstream format signals having a uniform word format;
 - 15 - means for further processing said PCM bitstream format signals so as to form therefrom sample words that are stored in an intermediate store, e.g. a FIFO, from which the sample words are fed to a central processing.
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4. Apparatus for pre-processing output signals for interfaces of different type in a common-format central processing using a common system clock, said different interface types being associated with differing sample clock frequencies and/or differing data frame or data word formats, said apparatus including:
- 25 - means for further processing sample words that were output from said central processing and stored in an intermediate store, e.g. a FIFO, by forming system clock synchronised PCM bitstream format signals therefrom, which PCM bitstream format signals have a uniform word format and are related to said interfaces of different type;
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- means for channel encoding said system clock synchronised PCM bitstream format signals having a uniform word format according to the differing channel protocols related to said different-type interfaces, thereby providing corresponding system clock synchronised output signals;
- means for generating from said system clock synchronised output signals interface-type related output signals that are no more system clock synchronised but conform to said type of interface.

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5. Method according to claim 1 or 2, wherein said interface types include at least two of IEC958, I2S, AC-Link and ADAT.

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6. Method according to claim 1 or 2, wherein some individual samples are marked or checked with their channel type in the system clock synchronised processing in order to detect and avoid channel permutation, said channel permutation occurring e.g. in case of insertion or deletion of samples, said marking being carried out e.g. by using subcode bits that are otherwise not used in said system clock synchronised processing.

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7. Method according to claim 1 or 2, wherein for DMA data block transfer in connection with said intermediate storage an LF marking is carried out for the first word of each DMA data block and is evaluated in order to reduce the number of processor operations when preparing a DMA buffer output.

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8. Method according to claim 1 or 2, wherein for facilitating a precisely timed start-up of a stream unit that performs said further processing of the sample words, an internally generated time stamp is supplied to the stream unit by the central processing.

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9. Method according to one of claims 1 to 8, wherein for
synchronisation of interface signals that have separate
clock and data or sync signals to said system clock, two
succeeding D flip-flops are used that are clocked by the
5 same edge of the clock to be synchronised.
5. Apparatus according to claim 3 or 4, wherein said inter-
face types include at least two of IEC958, I2S, AC-Link
and ADAT.
- 10 6. Apparatus according to claim 3 or 4, wherein some indi-
vidual samples are marked or checked with their channel
type in the system clock synchronised processing in order
to detect and avoid channel permutation, said channel
15 permutation occurring e.g. in case of insertion or dele-
tion of samples, said marking being carried out e.g. by
using subcode bits that are otherwise not used in said
system clock synchronised processing.
- 20 7. Apparatus according to claim 3 or 4, wherein for DMA data
block transfer in connection with said intermediate stor-
age an LF marking is carried out for the first word of
each DMA data block and is evaluated in order to reduce
the number of processor operations when preparing a DMA
25 buffer output.
8. Apparatus according to claim 3 or 4, wherein for facili-
tating a precisely timed start-up of a stream unit that
performs said further processing of the sample words, an
internally generated time stamp is supplied to the stream
30 unit by the central processing.
9. Apparatus according to claim 3 or 4, wherein for synchro-
nisation of interface signals that have separate clock
35 and data or sync signals to said system clock, two
succeeding D flip-flops are used that are clocked by the

same edge of the clock to be synchronised.